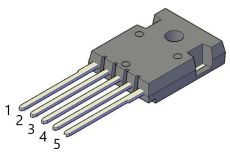
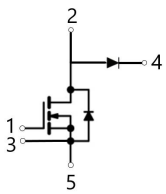
PFC Boost Module with N-channel Power MOSFET and SiC SBD

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ max. at 25°C (mΩ)	V_{GS}=10V	180
Vf max at at 25°C (SiC SBD)	If=10A	1.2V
Configuration	MOSFET+ SiC SBD	





Schematic diagram

1	MOS: Gate
2	Mos: Drain
	Diode: Anode
3	MOS: Driver Source
4	Diode: Cathode
5	MOS: Power Source

Features

- New Technology For PFC Module
- New package design with compliance to To-247 body dimensions but 5 pins
- Heatsink isolated to all pins
- ID=20A(Vgs=10V)
- RoHS Compliant

Applications

- High efficiency Power factor correction (PFC) design for Switching Mode Power Supplies (SMPS)

ORDERING INFORMATION	
Device	SP5A65R18010G
Device Package	TO-247-5
Marking	65R18010

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain to Source Voltage	V_{DSS}	650	V
Continuous Drain Current (@T_C=25°C)	I_D	20 (1)	A
Continuous Drain Current (@T_C=100°C)		13 (1)	A
Drain current pulsed (2)	I_{DM}	60 (1)	A
Gate to Source Voltage	V_{GS}	±30	V
Single pulsed Avalanche Energy (3)	E_{AS}	400	mJ
MOSFET dv/dt ruggedness (@V_{DS}=0~400V)	dv/dt	25	V/ns
Peak diode Recovery dv/dt (4)	dv/dt	15	V/ns
Total power dissipation (@T_C=25°C)	P_D		W
Derating Factor above 25°C		0.3	W/°C
Operating Junction Temperature & Storage Temperature	T_{STG}, T_J	-55 to + 150	°C
Maximum lead temperature for soldering purpose(5)	T_L	260	°C
Mounting torque (5)		0.4~0.6	N.m

Notes
1. Drain current is limited by maximum junction temperature.
2. Repetitive rating : pulse width limited by junction temperature.
3. L = 50mH, I_{AS} = 4A, V_{DD} = 50V, R_G=25Ω, Starting at T_J = 25°C
4. I_{SD} ≤ I_D, di/dt = 100A/us, V_{DD} ≤ 480V, Starting at T_J =25°C
5. Mounting consideration for TO220 Fullpack:
   M3 screw plus flat washer is suggested, free of burr between devices and contact area,
   the devices are to be mounted to a hole not larger than 3.6mm in contact diameter (chamfer included).

THERMAL CHARACTERISTICS			
Parameter	**Symbol**	**Value**	**Unit**
Thermal resistance, Junction to case	R_{thjc}	0.3	°C/W
Thermal resistance, Junction to ambient	R_{thja}	45	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Off Characteristics						
Drain to source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	--	--	V
Breakdown voltage temperature coefficient	ΔBV_{DSS} / ΔTJ	I_D=250uA, referenced to 25°C	--	0.7	--	V/°C
Drain to source leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		V_{DS}=650V, T_C=125°C	--	--	10	uA
Gate to source leakage current, forward	I_{GSS}	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
Gate to source leakage current, reverse		V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
On Characteristics						
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	2.5	3.5	4.5	V
Drain to source on state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D =10A	--	160	180	mΩ
Forward Transconductance	Gfs	V_{DS} = 20 V, I_D = 10A	--	14	--	S
Dynamic Characteristics						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=200V, f=1MHz	--	1996	--	pF
Output capacitance	C_{oss}		--	66	--	
Reverse transfer capacitance	C_{rss}		--	7.7	--	
Turn on delay time	$t_{d(on)}$	V_{DS}=380V, I_D=20A , R_G=18Ω, V_{GS}=10V	--	26	--	ns
Rising time	tr		--	46	--	
Turn off delay time	$t_{d(off)}$		--	86	--	
Fall time	t_f		--	31	--	
Total gate charge	Q_g	V_{DS}=520V, V_{GS}=10V, I_D=20A	--	58	72	nC
Gate-source charge	Q_{gs}		--	16.2	--	
Gate-drain charge	Q_{gd}		--	25	--	

SiC DIODE RATINGS CHARACTERISTICS						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Continuous forward current	I_F		--	--	10	A
Maximum forward current	I_{FM}		--	--	60	A
Diode forward voltage drop	Vf	If=10A	--	1.3	1.5	V
Reverse Breakdown Voltage	BV	Ir=100uA	650			V
Reverse leakage current	Ir	Bv=650V		5	30	uA

Fig1. Output characteristics

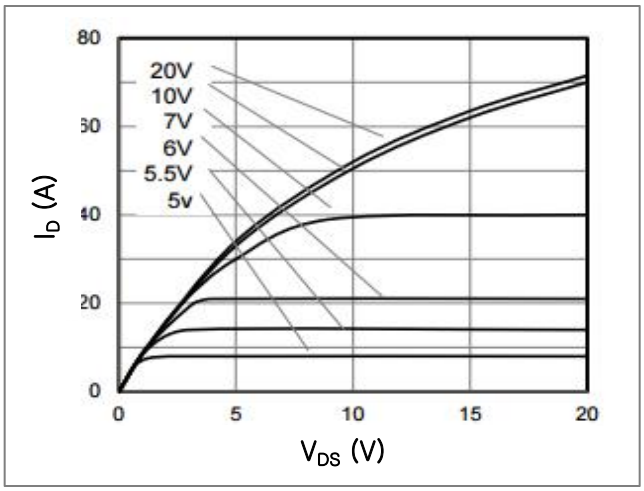


Fig2. On-Resistance vs. Drain Current

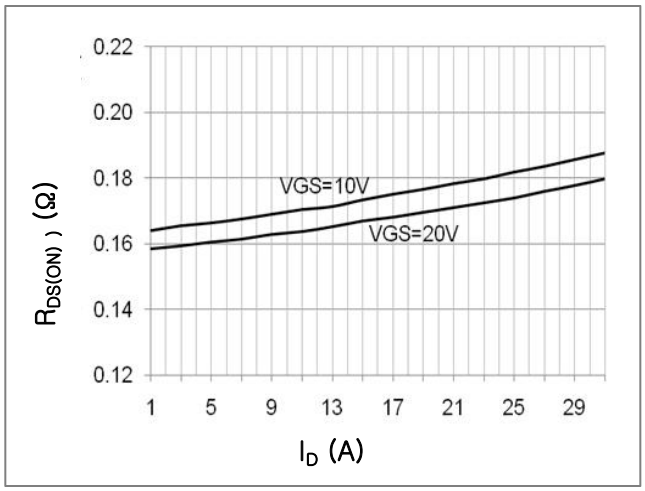


Fig3. Gate charge characteristics

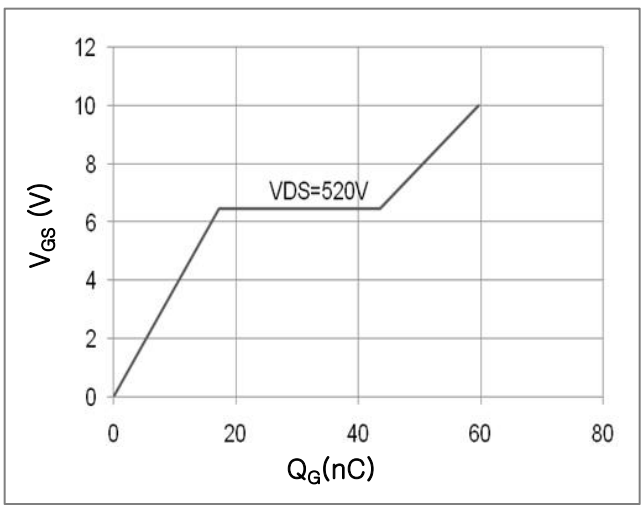


Fig 4. Capacitance Characteristics

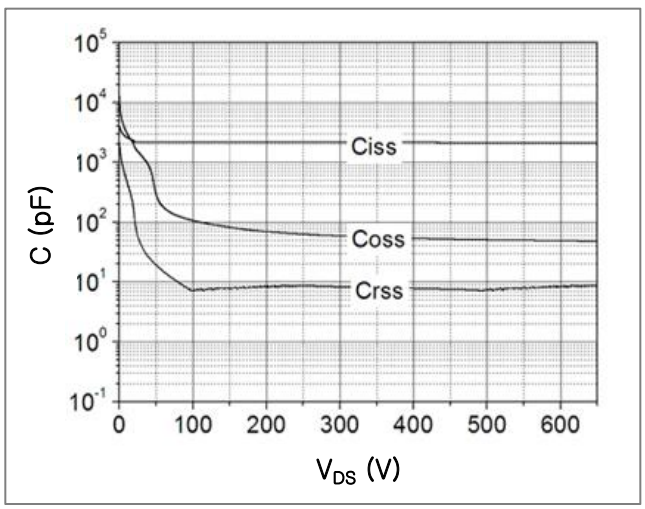


Fig 5. $R_{DS(ON)}$ vs junction temperature

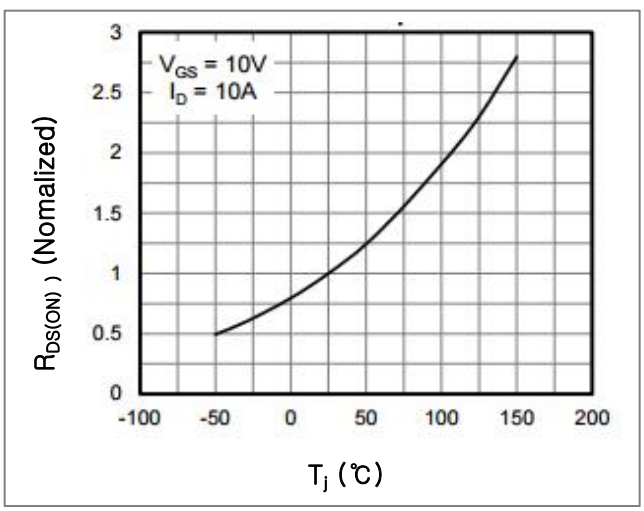


Fig 6. Threshold Voltage vs Junction Temperature

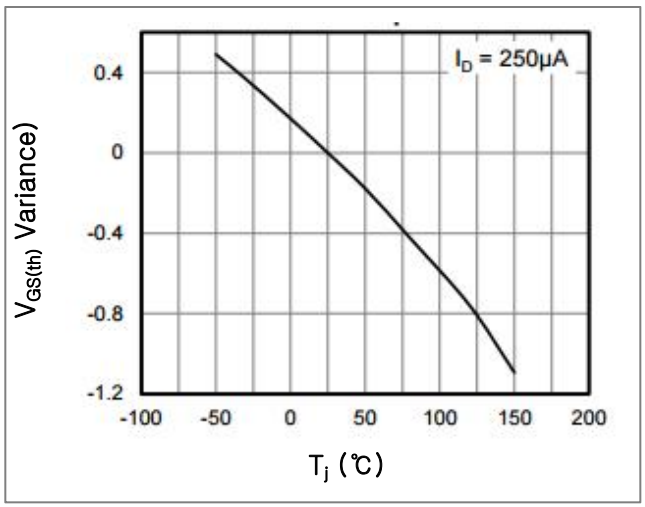


Fig 7 . Safe operating area

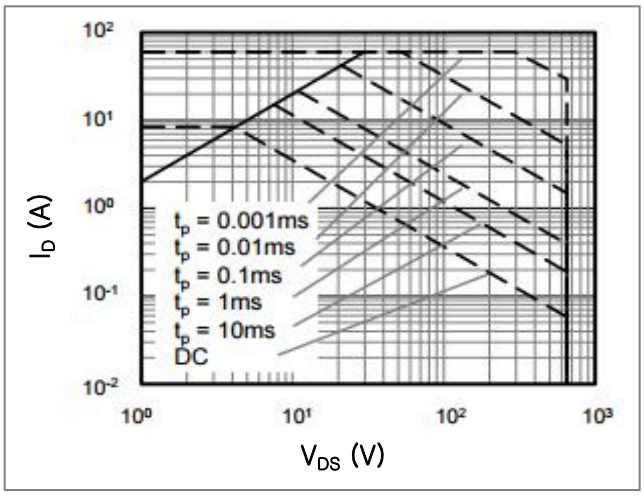


Fig 8 . Transient thermal impedance

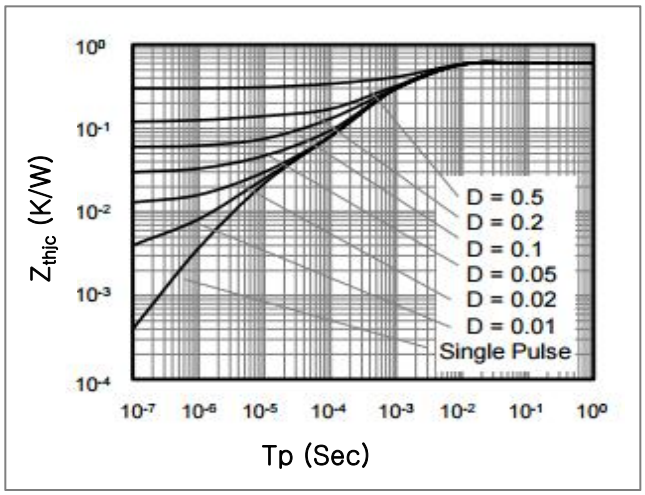


Fig 9. Forward characteristics of reverse diode

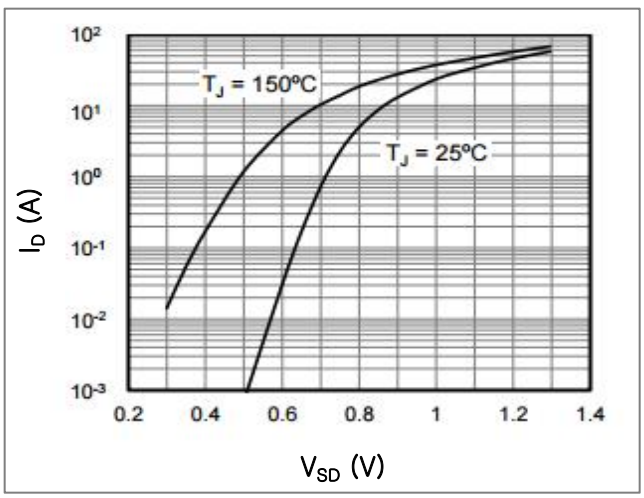


Fig 10 . Transfer characteristics

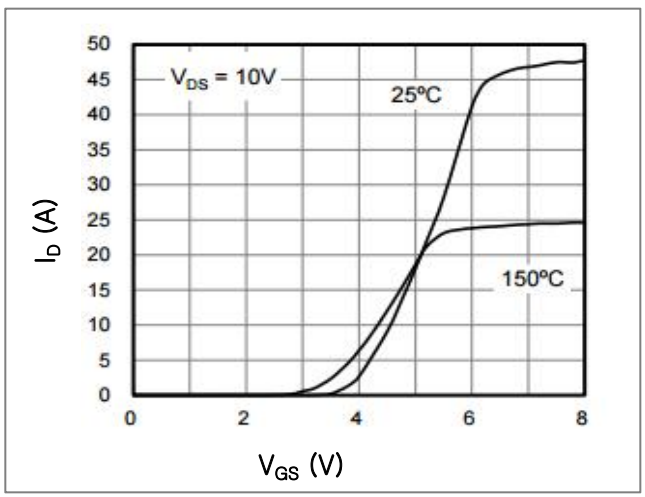
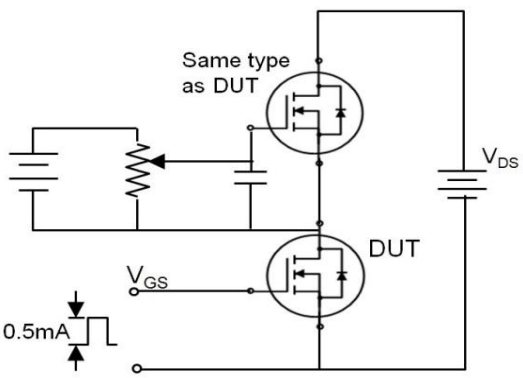


Fig 11. Gate charge test circuit & waveform



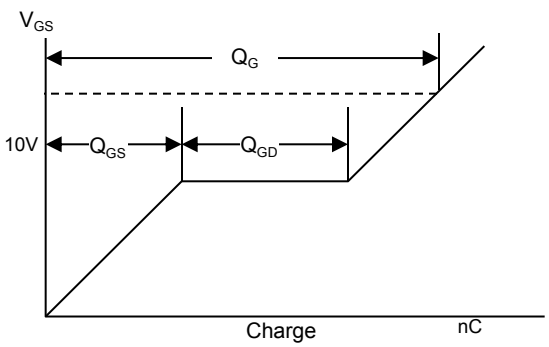


Fig 12. Switching time test circuit & waveform

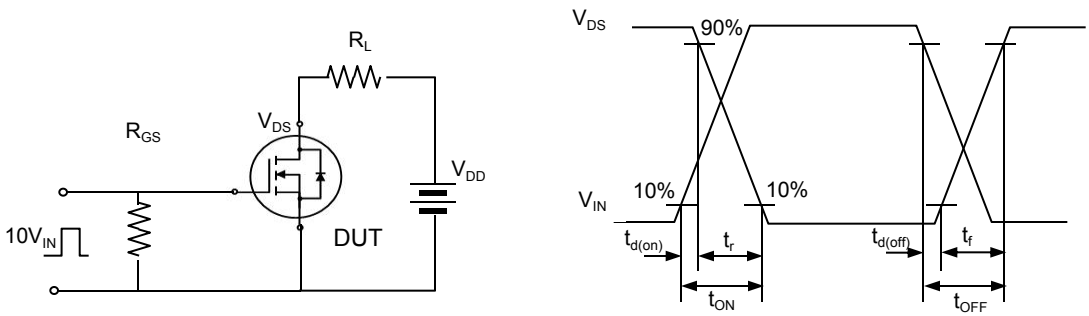


Fig 13. Unclamped Inductive switching test circuit & waveform

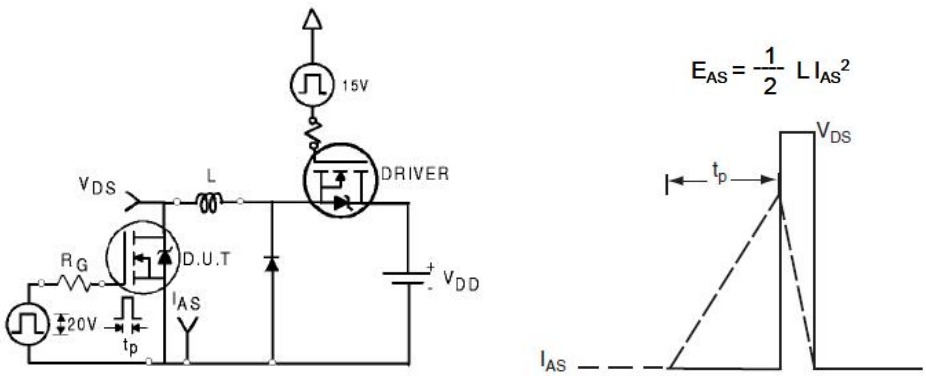
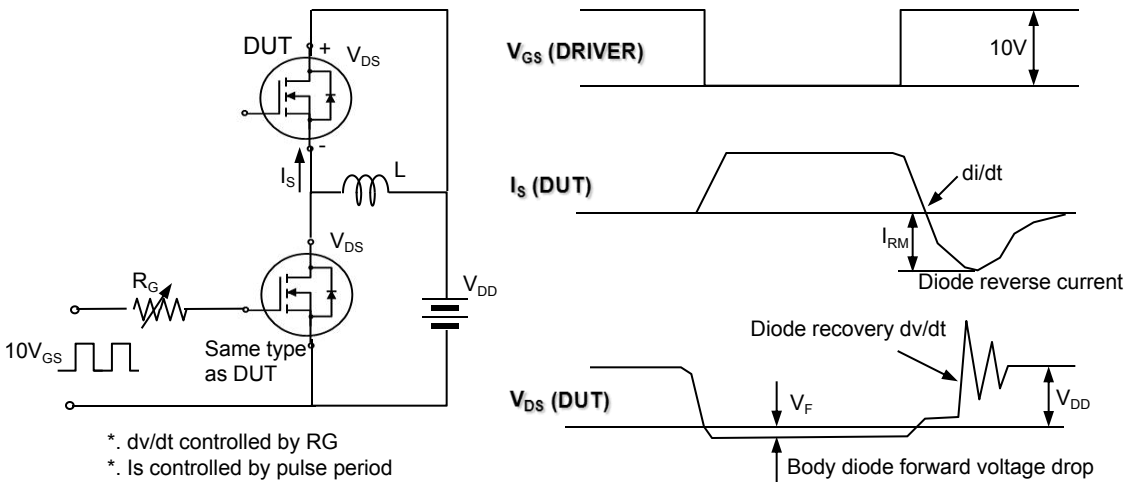


Fig 14. Peak diode recovery dv/dt test circuit & waveform



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